REMARKS

Present Status of the Application

The Office Action rejected presently-pending claims 1, 6-8, and 15 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Also, the Office Action rejected claims 1-4 and 9-17 under 35 U.S.C. 102(b), as being anticipated by Huang et al. (U.S. 5,761,479) ("Huang," hereinafter). Applicants have amended claims 1, 2, 3, 6, 9, 15 to improve clarity. After entry of the foregoing amendments, claims 1-17 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action indicated that claim 5 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate this indication of allowable subject matter.

The Office Action rejected claims 1, 6-8 and 15 under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.. Claims 1, 6-8 and 15 are amended for clarification. In view of the amendments, reconsideration and withdrawal of the Section 112 rejections is respectfully requested.

The Office Action also rejected claims 1-4 and 9-17 under 35 U.S.C. 102(b) as being anticipated by Huang et al. (U.S. 5,761,479). Applicants respectfully traverse the rejections for at least the following reasons.

For a proper rejection of a claim under 35 U.S.C. Section 102(b), the cited reference must disclose all elements/features/steps of the claim.

Independent Claim 1, as amended, states:

An apparatus for supporting multi-processors, wherein said apparatus is coupled to a central processing unit(CPU) socket, having a plurality of connecting pins, and when said CPU socket is inserted with a first type CPU, a first pin among said connecting pins has a first equivalent resistance, and when said CPU socket is inserted with a second type CPU, said ~~second~~ first pins has a second equivalent resistance, wherein the first equivalent resistance is not equal to the second equivalent resistance, said apparatus comprising:

a distinguish device, coupled to said first pin to ~~apply a~~ use difference between said first and said second equivalent resistances to generate a CPU select signal; and

a switch circuit, coupled to said distinguish device and said CPU socket to selectively connect a plurality of first type CPU signals to said corresponding connecting pins, and a plurality of second type CPU signals to said corresponding connecting pins according to ~~control a~~ status of said CPU select signal.

Independent claim 1 is allowable for at least the reason that Huang does not disclose, teach, or suggest the features that are highlighted in claim 1 above. More specifically, the present invention provides an apparatus and method for supporting different types of processors on a single motherboard. In order to achieve this objective, the present invention provides a

distinguish device that distinguishes a first type CPU from a second type CPU based on the resistances produced by the two CPUs when connected to a CPU socket.

As disclosed in the specification of the invention, the distinguish device 210 described in the present invention uses pins Z36 and AK36 of Socket-370 to determine the type of CPU connected to Socket-370. The distinguish device comprises ***a processor select circuit 200 and an interval control circuit 240***. When Coppermine type CPU is inserted on the motherboard, before the system is activated, the resistance of pin Z36 is larger than 100K and that of pin AK36 approaches zero. On the contrary, when Tualatin type CPU is inserted on the motherboard, the resistance of these two pins is almost the same and in the range of 20 to100 K. The processor select circuit uses the property of the two processors producing ***different resistance values at the same pin*** to distinguish which type of processor is connected to the Socket-370 ***before the system is activated***. (Page 6, Para 0019)

After distinguishing the type of processor connected to Socket-370 based on the difference in resistances of the processors, the processor select circuit 200 generates a CPU type select signal (C or T OUT). Depending on the type select signal a switch circuit 220 connects proper circuits to the Socket-370 CPU 120. In addition, the interval control circuit 240 generates a cutoff activate signal, transmitted to the processor select circuit 200, so as to cut off the connection between the processor select circuit 200 and the pins Z36 and AK36 of the Socket-370, after the CPU type signal has been generated. It thus ensures that the pins Z36 and AK36 are not affected by the processor select circuit 200 in normal operation of the system. (Page 7, Para 0020)

The cited reference Huang describes a system for supporting multiple CPUs on a motherboard. The patent describes a computer system 20 comprising ***a first socket 1001 for receiving a first processor and a second socket 1002 for receiving a second processor***. The cited reference further describes that a PIN B14 of the first socket 1001 is used to ***output a MP#***

signal if a 80487SX model is plugged in or is open (and tied to a high voltage through a resistor R1); ***when a 80468DX is plugged in***. (Column 20, lines 16-30)

Therefore the cited reference Huang differs from the present invention as it uses two different sockets for supporting two different processors. In addition, Huang does not describe that the two processors produce different resistances when they are connected to the same pins in a socket on the motherboard. The cited reference Huang also does not describe the use of the difference in resistances produced by the two processors in order to distinguish between them. Further, the cited reference Huang does not disclose an interval control circuit which generates a cutoff activate signal, being transmitted to a processor select circuit in order to cut off the connection between the processor select circuit and the pins Z36 and AK36 of the Socket-370, after the CPU type signal has been generated. Thus a circuit ensuring that the pins Z36 and AK36, which were used to distinguish between the two processors, are not affected by the processor select circuit in normal operation of the system.

To summarize, the cited reference Huang in the Office Action does not disclose or suggest a system and method for distinguishing between different processors connected to specific pins in a socket of a motherboard, based on the difference in resistances produced by the processors at the pins. The cited reference Huang discloses a circuit for identifying the model of a processor plugged in a socket. However, the identification is not described as being based on measuring the resistance generated by each plugged in processor and finding out the difference between the measured resistances. Therefore the present invention provides features that are not present in the prior art; when taken alone or in combination. The distinguishing features distinctly claimed in the present claims as amended are not rendered obvious by the prior art.

Thus, cited reference Huang does not anticipate claim 1, and the rejection should be withdrawn.

If independent claim 1 is allowable over the prior art of record, then its dependent claims 2-13 are allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 1. Additionally and notwithstanding the foregoing reasons for the allowability of claim 1, these dependent claims recite further features/steps and/or combinations of features/steps (as is apparent by examination of the claims themselves) that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-17 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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